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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,815	12/22/2000	Jean-Didier Allegrucci	3242P008	8894

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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,815	ALLEGRUCCI ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed May 20, 2003, in response to PTO Office Action dated February 20, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-15 have been presented for examination in this application. In response to the last Office Action, claims 1, 6, and 11 have been amended.

Claim Objections

Claims 6-10 are objected to because of the following informalities: Claim 10 recites "the external memory alias" in line 7. The Examiner believes that the claim language was intended to read –the internal memory alias--, in order to correspond to the "internal memory having an alias" recitation in lines 3-4, and will interpret the claim as such. Claims 7-10 are objected to as being dependent upon a previously object claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 10-13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virajpet et al. (US# 6,480,948), James, Jr. et al. (US# 6,240,519), and Cheung et al. (US# 6,262,594)

Regarding claims 6 and 11, Virajpet et al. teaches a system for memory aliasing ~~system~~. The processor is able to read from an internal ROM (31) for initialization (configuration) or boot code processing (col. 3, lines 1-16; col. 4, lines 5-23). Section (31) of the memory map is configurable, and during a first time period, the configurable section is aliased so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.

A first difference between the claimed subject matter and that of Virajpet et al., disclosed supra, is that the claim recites searching for a valid secondary initialization routine. James, Jr. et al. teaches a system for recovering from a corrupted boot ROM image. The ROM image is found within the ROM device, and once the processor determines that the image is corrupt, the processor continues to execute the boot block code of the ROM (col. 7, lines 54-58; col. 8, lines 4-12; Fig. 6A-6D). James, Jr. et al. teaches searching for a secondary init. routine in the form of determining if a floppy disk (external memory) is present in the floppy drive. If the diskette is present, the boot sequence is initialized from the floppy disk without the aid of the original ROM (col. 8,

line 53 – col. 9, line 1). Booting of the original ROM was disabled in order for the diskette boot sequence to occur.

Another difference between the claimed subject matter and that of Virajpet et al. and James, Jr. et al., is that the claims recite that the aliasing is done for a configurable system-on-chip system. Cheung et al. teaches a configurable system-on-chip design. According to Figure 4, which illustrates specific modules that may be incorporated onto a system-on-chip configuration, Cheung et al. teaches an external memory system coupled to the system-on-a-chip in the form of an external flash ROM (non-volatile memory) (col. 7, lines 56-60). Also, an erasable read-only-memory is taught for storing control values (col. 3, lines 14-16), where the ROM is found on the system-on-chip. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet et al., James, Jr. et al., and Cheung et al. before him at the time the invention was made to modify the aliasing system of Virajpet et al. to include the recoverable ROM system of James, Jr. et al. and the system-on-chip design of Cheung et al., because then a single integrated circuit chip would yield advantages of cost reduction, low power consumption, space savings and ruggedness, as taught by Cheung et al, as well as teach a system for reflashing a corrupted ROM for future use, as taught by James, Jr. et al.

Regarding claims 7 and 12, Virajpet et al. teaches loading initialization operations from an external non-volatile memory (flash) (col. 4, lines 9-13).

Regarding claims 8 and 13, the changing of aliases as taught by Virajpet et al. is done during a first time period following processor reset, such that the processor must re-initialize from the external memory (col. 3, lines 8-13).

Regarding claims 10 and 15, Virajpet et al. teaches a continuing program for the initialization program setup. As seen in Figure 3, should the select signal be set, the internal ROM is directed to return requested data (col. 5, lines 12-16).

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virajpet et al. (US# 6,480,948), James, Jr. et al. (US# 6,240,519), and Cheung et al. (US# 6,262,594)

Regarding claim 1, Virajpet et al. teaches a system for memory aliasing system. The processor is able to read from an internal ROM (31) for initialization (configuration) or boot code processing (col. 3, lines 1-16; col. 4, lines 5-23). Section (31) of the memory map is configurable, and during a first time period, the configurable section is aliased so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.

A first difference between the claimed subject matter and that of Virajpet et al., disclosed supra, is that the claim recites searching for a valid secondary initialization routine. James, Jr. et al. teaches a system for recovering from a corrupted boot ROM image. The ROM image is found within the ROM device, and once the processor

determines that the image is corrupt, the processor continues to execute the boot block code of the ROM (col. 7, lines 54-58; col. 8, lines 4-12; Fig. 6A-6D). James, Jr. et al. teaches searching for a secondary init. routine in the form of determining if a floppy disk (external memory) is present in the floppy drive. If the diskette is present, the boot sequence is initialized from the floppy disk without the aid of the original ROM (col. 8, line 53 – col. 9, line 1). Booting of the original ROM was disabled in order for the diskette boot sequence to occur.

Another difference between the claimed subject matter and that of Virajpet et al. and James, Jr. et al., is that the claims recite that the aliasing is done for a configurable system-on-chip system, as well as that the external memory is a flash memory. Cheung et al. teaches a configurable system-on-chip design. According to Figure 4, which illustrates specific modules that may be incorporated onto a system-on-chip configuration, Cheung et al. teaches an external flash ROM (non-volatile memory) with a flash ROM interface (col. 7, lines 56-60). Also, an erasable read-only-memory is taught for storing control values (col. 3, lines 14-16), where the ROM is found on the system-on-chip. One of ordinary skill in the art would recognize that the routines stored on the floppy diskette external memory of Jones, Jr. et al. could just as easily be stored and implemented in a secondary ROM device like that of Cheung et al. The system of James et al. uses floppy disk to store the boot initialization routine and flashing code in fact (col. 9, lines 8-12). Implementation of the secondary ROM device would negate the increased financial cost, as well as the increased system size, of a floppy disk drive. The Examiner takes Official Notice of these teachings. Therefore it would have been

obvious to one of ordinary skill in the art having the teachings of Virajpet et al., James, Jr. et al., and Cheung et al. before him at the time the invention was made to modify the aliasing system of Virajpet et al. to include the recoverable ROM system of James, Jr. et al. and the system-on-chip design of Cheung et al., because then a single integrated circuit chip would yield advantages of cost reduction, low power consumption, space savings and ruggedness, as taught by Cheung et al, as well as teach a system for reflashing a corrupted ROM for future use, as taught by James, Jr. et al.

Regarding claim 2, Virajpet et al. teaches loading initialization operations from an external non-volatile memory (flash) (col. 4, lines 9-13).

Regarding claim 3, the changing of aliases as taught by Virajpet et al. is done during a first time period following processor reset, such that the processor must re-initialize from the external memory (col. 3, lines 8-13).

Claims 4, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Virajpet et al. (US# 6,480,948), James, Jr. et al. (US# 6,240,519), Cheung et al. (US# 6,262,594), and Bartoli et al. (US# 6,401,164).

The difference between the claimed subject matter and that of Virajpet et al. (US# 6,480,948), James, Jr. et al. (US# 6,240,519), and Cheung et al. (US# 6,262,594), disclosed supra, is that the claims recite that code is executed in a manner starting from the bottom of the ROM memory. Bartoli et al. teaches both top and bottom boot sector configurations for an internal ROM device (Figures 1A & 1B; col. 1, line 49 – col. 2, line

19). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet et al., James Jr., et al., Cheung et al., and Bartoli et al. before him at the time the invention was made to modify the internal memory of Virajpet et al. , James Jr. et al., and Cheung et al. to include reading initialization code from the top or bottom of the memory, because then greater functionality for specific system designs could be incorporated that would take advantage of reading from either the top or bottom of the internal memory for initialization routines.

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant has argued, on page eight of the response filed May 20, 2003, that a configurable system-on-a-chip integrates a "CPU, an internal system bus,

programmable logic, and various system resources...". This argument is used to demonstrate that the Cheung reference is not a true system-on-a-chip. Also, the Applicant has argued that the system-on-a-chip of Cheung does not claim to be configurable, rather that the "use of the pads is configurable". The Examiner would like to point out that the claim limitations fail to recite each of the features the Applicant has stated are integrated into a system-on-a-chip. Also, reconfiguration of the system-on-a-chip could take many forms, such as the reflashing of the internal ROM as taught by James, Jr. et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to other secondary initialization schemes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

13/2/3
DS/BRP

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

July 2, 2003